AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (currently amended): An information storage system provided with a bulk memory and a host device for controlling writing of data into said bulk memory, said host device comprising:

an NG table for storing addresses ~~specifying areas~~ of said bulk memory and information showing whether or not data can be written into an area of said bulk memory specified by an address~~into which data cannot be written~~;

a performance-guaranteed environment determination means for determining whether or not a current environment of said bulk memory is outside a performance-guaranteed environment in which performance of said bulk memory is guaranteed; and

a control means for writing data in an area of said bulk memory specified by ~~an~~ a writable address of ~~which is not stored in~~ said NG table when said performance-guaranteed environment determination means determines that the current environment is outside the performance-guaranteed environment.

2. (currently amended): The information storage system according to claim 1, wherein said control means includes:

an address acquisition means for acquiring the writable address of said ~~bulk memory which is not stored in said~~ NG table when said performance-guaranteed environment determination means determines that the current environment of said bulk memory is outside the performance-guaranteed environment;

a data acquisition means for acquiring the data which are to be written into said bulk memory;

a data writing means for writing the data acquired by said data acquisition means into the area of said bulk memory which is specified by the writable address acquired by said address acquisition means; and

a verification checking means for comparing the data which have been written into the area by said data writing means with the data acquired by said data acquisition means, and for ~~writing~~ generating information in said NG table indicating that data cannot be written to the area of the bulk memory specified by the writable address acquired by said address acquisition means ~~in said NG table~~ when determining that the data which have been written into the area does not match the data acquired by said data acquisition means.

3. (currently amended): The information storage system according to claim 2, wherein said address acquisition means makes a request of a file system that manages files stored

in said bulk memory to acquire the writable address ~~which is not stored in said NG table so as to acquire the address of said bulk memory~~ from said file system.

4. (previously presented): The information storage system according to claim 2, wherein said data acquisition means acquires the data from a memory on a cluster-by-cluster basis.

5. (currently amended): The information storage system according to claim 1, wherein information indicating the addresses specifying areas of said bulk memory into which data cannot be written ~~are~~ is stored in said NG table if an attempt, by said control means, to write data in said areas is unsuccessful and wherein the host device is a separate device from the bulk memory.

6. (previously presented): The information storage system according to claim 2, wherein if said verification checking means determines that the data which have been written into the area does not match the data acquired by said data acquisition means, the data writing means rewrites the data acquired by said data acquisition means into an area of said bulk memory which is specified by a different address.

7. (previously presented): The information storage system according to claim 6, wherein if a number of attempts to write the data acquired by said data acquisition means into said bulk memory exceeds a permissible number of times, the verification checking means generates an error event.

8. (currently amended): A host device for controlling writing of data into a bulk memory, said host device comprising:

an NG table for storing addresses ~~specifying areas~~ of said bulk memory and information showing whether or not data can be written into an area of said bulk memory specified by an address~~into which data cannot be written~~;

a performance-guaranteed environment determination circuit which determines whether or not a current environment of said bulk memory is outside a performance-guaranteed environment in which performance of said bulk memory is guaranteed; and

a control circuit which writes data in an area of said bulk memory specified by ~~an~~ a writable address ~~which is not stored in~~ of said NG table if said performance-guaranteed environment determination circuit determines that the current environment is outside the performance-guaranteed environment.

9. (currently amended): The host device according to Claim 8, wherein said control circuit comprises:

an address acquisition circuit which acquires the writable address of said ~~bulk memory which is not stored in said~~ NG table if said performance-guaranteed environment determination circuit determines that the current environment of said bulk memory is outside the performance-guaranteed environment;

a data acquisition circuit which acquires the data which are to be written into said bulk memory, a data writing circuit which writes the data acquired by said data acquisition circuit into the area of said bulk memory which is specified by the writable address acquired by said address acquisition circuit; and

a verification checking circuit which compares the data which have been written into the area by said data writing circuit with the data acquired by said data acquisition circuit, and for ~~writing~~ generating information in said NG table indicating that data cannot be written to the area of the bulk memory specified by the writable address acquired by said address acquisition circuit in said NG table if determining that the data which have been written into the area does not match the data acquired by said data acquisition circuit.

10. (currently amended): The host device according to claim 9, wherein said address acquisition circuit makes a request of a file system that manages files stored in said bulk memory

to acquire the writable address ~~which is not stored in said NG table so as to acquire the address of said bulk memory~~ from said file system.

11. (previously presented): The host device according to claim 9, wherein said data acquisition circuit acquires the data from a memory on a cluster-by-cluster basis.

12. (currently amended): The host device according to claim 8, wherein information indicating the addresses specifying areas of said bulk memory into which data cannot be written ~~are~~ is stored in said NG table if an attempt, by said control circuit, to write data in said areas is unsuccessful and wherein the host device is a separate device from the bulk memory.

13. (previously presented): The host device according to claim 9, wherein if said verification checking circuit determines that the data which have been written into the area does not match the data acquired by said data acquisition circuit, the data writing circuit rewrites the data acquired by said data acquisition circuit into an area of said bulk memory which is specified by a different address.

14. (previously presented): The host device according to claim 13, wherein if a number of attempts to write the data acquired by said data acquisition circuit into said bulk

memory exceeds a permissible number of times, the verification checking circuit generates an error event.